REMARKS

In paragraph 3 of the Action, claims 1-6, 8-11, 14-19 and 21-24 were rejected under 35 U.S.C. 112, second paragraph. In paragraph 5 of the Action, claims 1-5, 8, 10, 11, 14-18, 21, 23 and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Miyazaki. In paragraph 6 of the Action, claims 6 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Miyazaki and Megiddo.

In view of the rejections, claims pending in the application have been canceled, and new claims 27-30 have been filed.

In claim 27, a motion picture encoding or decoding system for sequentially encoding or decoding a motion picture as a unit, the unit being formed of a plurality of successive frames, comprises:

necessary operation volume calculating means for calculating an operation volume necessary for encoding or decoding a present frame,

deciding means for deciding operating power-supply voltage - substrate bias voltage - operating frequency, said deciding means deciding the operating frequency capable of encoding or decoding the operation volume necessary for encoding or decoding the present frame within a time allocated in advance, and the operating power-supply voltage and the substrate bias voltage corresponding to the operation frequency, and

a processor implemented with MOS transistors laminated on a semiconductor substrate, the processor controlling the operating power-supply voltage, the operating frequency and the substrate bias voltage.

In the invention, the processor selects an actual operating frequency exceeding the necessary operating frequency within an operable frequency and most close to the operating frequency, and decides an actual operating power-supply voltage and an actual substrate bias voltage to make a power consumption minimum to the

selected frequency. The processor operates steadily in the present frame with the actual substrate bias voltage, the actual operating power-supply voltage and the actual operating frequency decided by the deciding means while the encoding or decoding means encodes or decodes the present frame.

Choi discloses a dynamic voltage and frequency scaling technique for MPEG decoding to reduce the energy consumption. The computational workload for an incoming frame is predicted using a frame-based history so that the processor voltage and frequency can be scaled to provide the exact amount of computing power needed to decode the frame. In the DVFS scheme, the frame-independent part is used to compensate for the prediction error that may occur during the frame-dependent part such that a significant amount of energy is saved.

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Choi does not disclose or suggest that the processor selects an actual operating frequency within the operable frequency, and decides the actual operating power-supply voltage and the actual substrate bias voltage. Claims of the invention are not disclosed or suggested by Choi.

Miyazaki is directed to a semiconductor integrated circuit including control circuits that generate the optimum clock signal, supply voltage and substrate bias. The operation can suppress the

variations of a CMOS circuit characteristic, and improve the circuit performance.

In Miyazaki, a bias voltage can be suppressed, but in the invention, the processor selects an actual operating frequency exceeding the necessary operating frequency within an operable frequency and most close to the operating frequency, and decides an actual operating power-supply voltage and an actual substrate bias voltage to make a power consumption minimum to the selected frequency. Thus, the processor controls the bias voltage as well as the operating power-supply voltage, so that it is possible to suppress the sub-threshold leak current, charging-discharging current and other leak currents. Accordingly, in the invention, the consuming power can be effectively reduced. Miyazaki does not disclose or suggest the features of the invention.

Megiddo was cited to disclose adding safe margin to hard disk seek and setting time in order to avoid failure in the case of underestimation of seek time. Actually, the disc scheduling or command sorting algorithm sorts pending disk I/O commands into a disk scheduling queue according to the time necessary to reach the position on the disk indicated by the command. In the invention, the processor selects the actual operating frequency exceeding the necessary operating frequency within the operable frequency, and decides the actual operating power-supply voltage and the actual substrate bias voltage. Megiddo is different in the field of invention, and does not disclose or suggest the features of the invention.

Zhao is directed to a macroblock classification for complexity management of a video encoder, wherein macroblocks are skipped during encoding of video date by algorithm that predicts the occurrence of skipped macroblocks prior to encoding. Although Zhao discloses the system to predict the occurrence of skipped

macroblocks, Zhao does not disclose or suggest the features of the invention now claimed.

As explained above, the cited references do not disclose or suggest the features of the invention now claimed. Even if the cited references are combined, claims of the application are patentable over the cited references.

Reconsideration and allowance are earnestly solicited.

Respectfully Submitted,

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